REMARKS

The Notice of Allowability, Form PTO-37, incorrectly lists the allowed claims as claims 1-33, 35, 36, 38-42,52, and 52. The allowed claims should be 1-3, 5-33, 35-36, 38-42, and 52-53.

This amendment corrects errors in the text. Entry is respectfully solicited. This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,

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Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

A marked-up version of the amended title, highlighting the changes thereto, follows to clearly identify the amendments:

FLEXIBLE BALL GRID ARRAY CHIP SCALE PACKAGES
[AND METHODS OF FABRICATION]

IN THE SPECIFICATION:

A marked-up version of paragraphs **[0003]**, **[0010]**, **[0024]**, and **[0038]**, highlighting the changes thereto, follows:

[0003] One type of integrated circuit (IC) or semiconductor die package is referred to as a "chip scale package," [,] "chip size package," [,] or merely "CSP." These designations arise largely from the physical dimensions of the package, which are only nominally larger than the actual dimensions (length, width and height) of the unpackaged semiconductor die. Chip scale packages may be fabricated in "uncased" or "cased" configurations. Uncased chip scale packages do not include an encapsulation or other covering of the sides of the semiconductor die extending between the active surface and back side thereof and, thus, exhibit a "footprint" (peripheral outline) that is substantially the same as that of an unpackaged semiconductor die. Cased chip scale packages have encapsulated or covered sides and thus exhibit a peripheral outline that is slightly larger than that of an unpackaged semiconductor die. For example, a surface area of a footprint for a conventional cased chip scale package may be up to about 1.2 times that of the bare semiconductor die contained within the package.

[0010] In one embodiment of the invention, the interposer substrate is little more than twice the size (footprint) of a bare semiconductor die to be packaged. The interposer substrate includes a first portion substantially of die footprint size and having a first set of contacts arranged for attachment to at least some of the bond pads on an active surface of the semiconductor die and a second portion laterally offset from the first portion by a spacer portion and bearing a second set of contacts arranged in an array, the interposer substrate including circuit traces extending between the first and second sets of contacts. A third set of contacts arranged in an array, with traces extending thereto from the first set of contacts, may optionally be located for access on the side of the first portion opposite the first set of contacts. The first set of contacts of the first portion of the interposer substrate is mechanically and electrically connected to the bond pads, which are preferably bumped with a conductive material, by any suitable technique known in the art, after which the second portion of the interposer substrate is

folded or wrapped around a side edge of the semiconductor die and adhesively attached to the back side of the semiconductor die. A dielectric underfill may optionally be disposed between the first portion of the interposer substrate and the active surface of the semiconductor die. Discrete conductive elements such as, by way of example only, solder balls, may be formed on the second set of contacts lying over the back side of the semiconductor or, if the interposer substrate employs the third set of contacts, either the second or third set of contacts may be so bumped, as desired. If both second and third sets of [contact] contacts are provided, multiple chip scale packages according to this embodiment of the invention may be stacked.

[0024] FIG. 1(a) also illustrates a cut-out from the interposer substrate 130 depicting the internal electrical interconnection or trace routings therein over one of the dielectric films thereof, the other being partially removed for clarity. In particular, the ball pads 135 on the second surface 134 of the interposer substrate 130 interconnect through conductive traces 144 to corresponding bond posts 143 exposed on the first surface 132 of first portion 136. Each bond post 143 is electrically connected and rerouted by way of a corresponding trace 144 to two corresponding ball pads 135 on the second surface 134 of the carrier substrate 130, one on first portion 136 and one on second portion 138. Traces 144 may be formed by masking and etching a conductive film, such as copper, on one of the dielectric films, by printing using conductive ink, or otherwise as known in the art. Bond posts 143 are formed of a conductive material compatible for bonding with bumps [116] 116b. Although actually sandwiched between the two dielectric films of interposer substrate 130, traces 144 are shown partially revealed from the side in FIGS. 1(b) and 1(c) and partially in broken lines to better illustrate their extensions from bond posts 143 to ball pads 135.

[0038] FIG. 3(b) is a simplified cross-sectional view of the first and second dice 110a and 110b attached to an interposer substrate 230. The first and second dice 110 may be attached to first portion 236 of interposer substrate 230 employing the same processes as discussed with respect to the first embodiment, either simultaneously or sequentially. As shown in FIG. 3(a), interposer substrate 230 is structured in a manner similar to that of interposer substrate 130,

being a laminate of two dielectric films having conductive traces 144 extending therebetween. However, conductive traces 144 of interposer substrate 230 extend from metallization pads 242 to an array of conductive pads through vias 235 extending from a first surface 232 of interposer substrate 230 to a second, opposing surface 234.